

# **P-Channel Power MOSFET**

-30V, -3A, 60mΩ

#### **Features**

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low Onresistance
- Pb-free plating
- RoHS compliant
- Halogen-free package

# **Application**

- Load Switch
- PA Switch

KEY PERFORMANCE PARAMETERS				
PARAMETER		VALUE	UNIT	
$V_{DS}$		-30	V	
R <sub>DS(on)</sub> (max)	V <sub>GS</sub> = -10V	60	mΩ	
	V <sub>GS</sub> = -4.5V	90		
$Q_g$		9.52	nC	





P-Channel MOSFET

#### **SOT-23**



Notes: Moisture sensitivity level: level 3. Per J-STD-020

ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	-30	V	
Gate-Source Voltage		$V_{GS}$	±20	V	
Continuous Drain Current (Note 1)	T <sub>A</sub> = 25°C	I <sub>D</sub>	-3	Α	
Pulsed Drain Current (Note 2)		I <sub>DM</sub>	-10	Α	
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	-1.9	Α	
Tatal Davian Discipation	T <sub>A</sub> = 25°C	Б	1.25	14/	
Total Power Dissipation	T <sub>A</sub> = 70°C	P <sub>DTOT</sub>	0.8	W	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	- 55 to +150	°C	

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	LIMIT	UNIT	
Junction to Case Thermal Resistance	R <sub>eJC</sub>	75	°C/W	
Junction to Ambient Thermal Resistance	R <sub>eJA</sub>	100	°C/W	

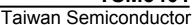
Notes: ReJA is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins. Reja is guaranteed by design while Reca is determined by the user's board design.  $R_{\theta JA}$  shown below for single device operation on FR-4 PCB in still air.



PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
Static (Note 3)	I	l		•		l
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	BV <sub>DSS</sub>	-30			V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	$V_{GS(TH)}$	-1.0	-1.5	-3.0	V
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I <sub>GSS</sub>			±100	nA
Zero Gate Voltage Drain Current	$V_{DS} = -24V, V_{GS} = 0V$	I <sub>DSS</sub>			-1	μA
On-State Drain Current	V <sub>DS</sub> = -5V, V <sub>GS</sub> = -10V	I <sub>D(ON)</sub>	-6			Α
	$V_{GS} = -10V, I_D = -3A$	_		50	60	mΩ
Drain-Source On-State Resistance	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -2A	$R_{DS(ON)}$		75	90	
Forward Transconductance	$V_{DS} = -15V, I_{D} = -5A$	g <sub>fs</sub>	4	7		S
Dynamic (Note 4)						
Total Gate Charge		$Q_g$		9.52		
Gate-Source Charge	$V_{DS} = -15V, I_D = -3A,$ $V_{GS} = -10V$	$Q_{gs}$		3.43		nC
Gate-Drain Charge		$Q_{gd}$		1.71		
Input Capacitance	45,4,4	C <sub>iss</sub>		551.57		
Output Capacitance	$V_{DS} = -15V, V_{GS} = 0V,$ f = 1.0MHz	C <sub>oss</sub>		90.96		pF
Reverse Transfer Capacitance	1 - 1.0IVITZ	C <sub>rss</sub>		60.79		
Switching (Note 5)						
Turn-On Delay Time		t <sub>d(on)</sub>		10.8		
Turn-On Rise Time	$V_{DD} = -15V,$ $R_{GEN} = 6\Omega,$ $I_{D} = -1A, V_{GS} = -10V,$	t <sub>r</sub>		2.33		
Turn-Off Delay Time		t <sub>d(off)</sub>		22.53		ns
Turn-Off Fall Time	1D - 1M, VGS - 10V,	t <sub>f</sub>		3.87		
Source-Drain Diode (Note 3)						
Forward On Voltage	I <sub>S</sub> = -1.9 A, V <sub>GS</sub> = 0V	$V_{SD}$		-0.8	-1.3	V

### Notes:

- 1. Pulse width limited by the maximum junction temperature.
- 2. Surface Mounted on FR4 Board,  $t \le 5$  sec.
- 3. Pulse test: PW  $\leq$  300 $\mu$ s, duty cycle  $\leq$  2%.
- 4. For DESIGN AID ONLY, not subject to production testing.
- 5. Switching time is essentially independent of operating temperature.





### **ORDERING INFORMATION**

PART NO.	PART NO. PACKAGE PACKING	
TSM3401CX RFG	SOT-23	3,000pcs / 7" Reel

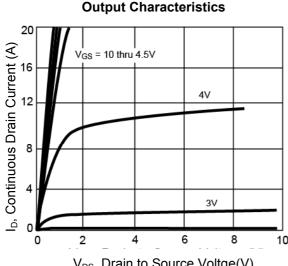
### Note:

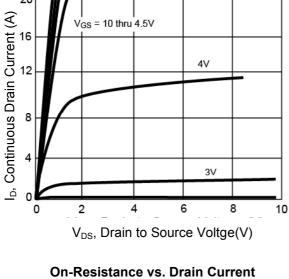
- 1. Compliant to RoHS Directive 2011/65/EU and in accordance to WEEE 2002/96/EC
- 2. Halogen-free according to IEC 61249-2-21 definition

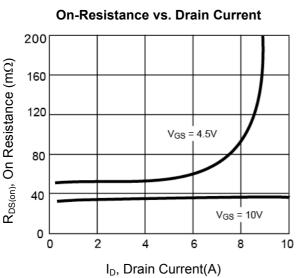


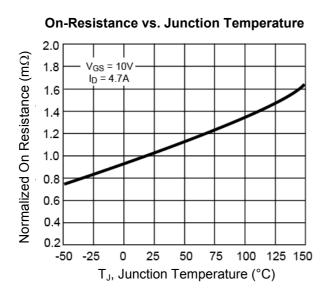
### **CHARACTERISTICS CURVES**

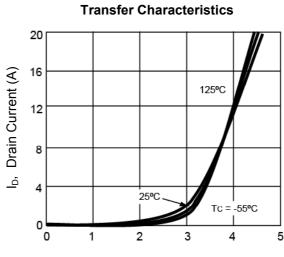
 $(T_A = 25^{\circ}C \text{ unless otherwise noted})$ 



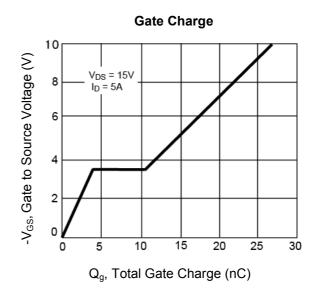




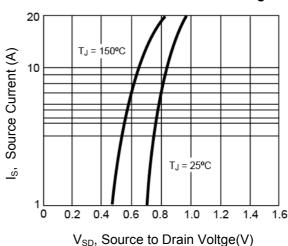




V<sub>GS</sub>, Gate to Source Voltge(V)



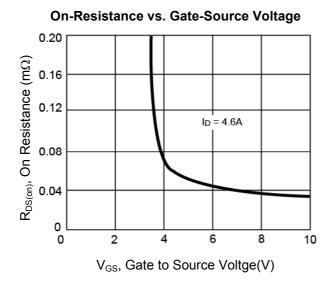
Source-Drain Diode Forward Voltage

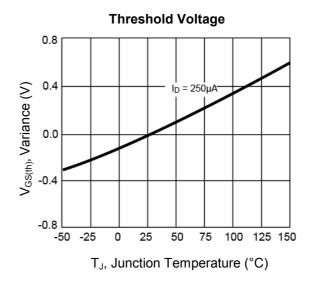


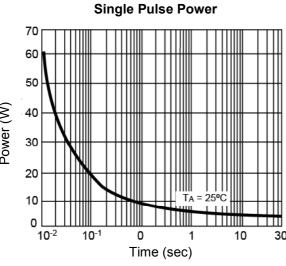


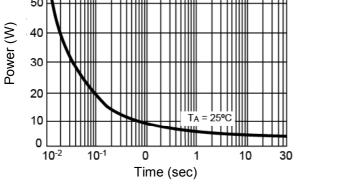
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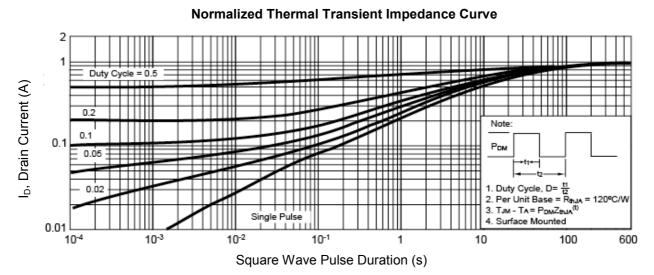
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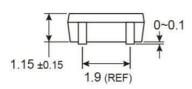


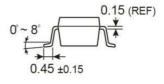




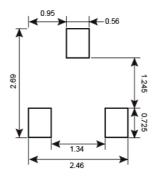


# PACKAGE OUTLINE DIMENSIONS (Unit: Millimeters)





### SUGGESTED PAD LAYOUT (Unit: Millimeters)



### **MARKING DIAGRAM**



Y = Year Code

**M** = Month Code for Halogen Free Product

O =Jan P =Feb Q =Mar R =Apr S =May T =Jun U =Jul V =Aug

W =Sep X =Oct Y =Nov Z =Dec

**L** = Lot Code (1~9, A~Z)



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